REMARKS

Claims 1-10, 13, 16, 18-28, 31, 34, 36-43, 45, 48, and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu, *et al.* (U.S. Patent Number 6,461,955) in view of Aoi (U.S. Patent Number 6,387,824) and Lee, *et al.* (U.S. Patent Number 6,171,951). Claims 17, 35 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu, *et al.* in view of Aoi, and Lee, *et al.* and further in view of Robinson, *et al.* (U.S. Patent Number 4,201,579). Claims 11-12, 14-15, 29-30, 32-33, 44 and 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu, *et al.* in view of Aoi and Lee, *et al.*, and further in view of Lui (U.S. Patent Number 6,391,761). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention of claims 1-20, a method of fabricating dual damascene interconnections includes forming an organo silicate glass layer on a substrate, and forming a via in the organo silicate glass layer. The via formed in the organo silicate glass layer is filled with a carbon-free inorganic filler. The method further includes processing the surface of the carbon-free inorganic filler filling the via formed in the organo silicate glass layer using plasma, and partially etching the inorganic filler filling the via and the dielectric layer to form a trench, which is connected to the via and in which interconnections will be formed.

In the present invention of claims 21-38, a method of fabricating dual damascene interconnections includes forming an organo silicate glass layer on a substrate, and forming a via in the organo silicate glass layer. The via formed in the organo silicate glass layer is filled with an HSQ-based filler. The method further includes processing the surface of the HSQ-based filler filling the via formed in the organo silicate glass layer using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate glass layer to form a trench, which is connected to the via and in which interconnections will be formed.

In the present invention of claims 39-52, a method of fabricating dual damascene interconnections includes forming a lower interconnection on a substrate and forming an etch stop on the lower interconnection. The method further includes forming an organo silicate glass layer on the etch stop layer and forming a via through the organo silicate glass layer to expose the

etch stop. The via is filled with an HSQ-based filler. The surface of the HSQ-based layer filling the via formed through the organo silicate layer is processed using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate glass layer to form a trench, which is connected to the via and in which interconnections will be formed.

Tsu, *et al.* discloses depositing a via protect layer 114 to fill a via. With reference to FIG. 2C of Tsu, *et al.*, after depositing the via protect layer 114, the via protect layer 114 is selectively etched back. A trench pattern 120 is then formed on a hardmask layer 110 and an IMD layer 108 and the via protect layer 114 filling the via are etched. IMD layer 108 is formed of a fluorine-doped silicate glass (FSG). FSG is a inorganic compound.

It is stated in the Final Office Action dated November 15, 2005 at page 3, lines 8-11, that Tsu, *et al.* fails to disclose an organo silicate glass and the value of its dielectric constant and processing the surface of the filler using plasma and the details about the plasma. Therefore, Tsu, *et al.* fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in an organo silicate layer using plasma, as claimed in claims 1-20. Tsu, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes partially etching the inorganic filler filling the via and the organo silicate layer to form a trench, as claimed in claims 1-20. Instead, in Tsu, *et al.*, the FSG layer 108 is an inorganic compound, while the claimed organo silicate layer is an organic compound. Therefore, when the carbon free inorganic filler and the organo silicate layer of the present invention are etched, there is a higher etch selectivity than in Tsu, *et al.* in which the via protect layer 114 and the FSG layer 108 are etched.

Tsu, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, as claimed in claims 21-38. Tsu, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 21-38. Instead, in Tsu, *et al.*, the FSG layer 108 is an inorganic compound, while the organo silicate layer is an organic compound. Therefore, when the HSQ-based filler

and the organo silicate layer of the present invention are etched, there is a higher etch selectivity then in Tsu, *et al.* in which the via protect layer 114 and the FSG layer 108 are etched.

Tsu, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, as claimed in claims 39-52. Tsu, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 39-52. Instead, in Tsu, *et al.*, the FSG layer 108 is an inorganic compound, while the organo silicate layer is an organic compound. Therefore, when the HSQ-based filler and the organo silicate layer of the present invention are etched, there is a higher etch selectivity then in Tsu, *et al.* in which the via protect layer 114 and the FSG layer 108 are etched.

Aoi discloses a resist pattern 12 formed having an opening over a region of an organic-inorganic hybrid film 11 to be used as a mask to form a wire groove or contact hole in the organic-inorganic hybrid film 11. However, Aoi does not teach or suggest a organo silicate layer. Therefore, Aoi fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, and partially etching the inorganic filler filling the via and the organo silicate layer to form a trench, as claimed in claims 1-20. Aoi further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 21-38. Aoi further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 39-52.

It is stated in the Advisory Action that whether the low-k dielectric is used as a filler or as an interlevel dielectric, the problems associated with the low-k dielectric material are still the same and methods of correcting or preventing these problems should be the same. In the present

invention, the plasma process is used in order to prevent a photoresist developing solution from dissolving the carbon-free filler or HSQ-based filler. The problem of the dissolution of the carbon-free filler or HSQ-based filler in processing, is not disclosed in Lee, *et al.*, instead, in Lee, *et al.*, the low-k dielectric prevents damage caused by subsequent processing. Damage done on low-k dielectric material resulting in lack of accurate control of feature dimensions, as disclosed in Lee, *et al.*, is not the same as dissolution of the carbon-free filler or HSQ-based filler in processing as disclosed in the present invention. Therefore, in the present invention as claimed in claims 1-52, the carbon-free filler or HSQ-based filler is not plasma treated for the purpose of having better control of feature dimensions as suggested by the Examiner in Advisory Action, but rather to prevent dissolution of the carbon-free filler or HSQ-based filler. Therefore, the teaching of plasma treating the surface of a low-k dielectric used as an interlevel dielectric, as disclosed in Lee, *et al.* is not usable for the carbon-free filler or HSQ-based filler.

Therefore, Lee, *et al.* fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, and partially etching the inorganic filler filling the via and the organo silicate layer to form a trench, as claimed in claims 1-20. Lee, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 21-38. Lee, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 39-52.

Tsu, *et al.*, Aoi and Lee, *et al.* fail to teach or suggest these elements of the invention set forth in claims 1-20, 21-28, and 39-52. Specifically, none of the references teaches or suggests a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma and partially

etching the inorganic filler filling the via and the organo silicate layer to form a trench, as claimed in claims 1-20, a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 21-38, or a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 39-52. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-20, 21-28, and 39-52. Therefore, it is believed that the claims 1-20, 21-28, and 39-52. are allowable over the cited references, and reconsideration of the rejections of claims 1-10, 13, 16, 18-28, 31, 34, 36-43, 45, 48, and 50-52 under 35 U.S.C. § 103(a) based on Tsu, *et al.*, Aoi and Lee, *et al.*, is respectfully requested.

Robinson, *et al.* is cited in the Office Action as disclosing the use of H_2-based plasma to remove photoresist. Robinson, *et al.* fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, and partially etching the inorganic filler filling the via and the organo silicate layer to form a trench, as claimed in claims 1-20. Robinson, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 21-38. Robinson, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 39-52.

Robinson, *et al.*, like Tsu, *et al.*, Aoi and Lee, *et al.*, fails to teach or suggest these

elements of the invention set forth in claims 1-20, 21-28, and 39-52. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-20, 21-28, and 39-52. Therefore, it is believed that the claims 1-20, 21-28, and 39-52. are allowable over the cited references, and reconsideration of the rejections of claims 17, 35 and 49 under 35 U.S.C. § 103(a) based on Tsu, *et al.*, Aoi, Lee, *et al.*, and Robinson, *et al.*, is respectfully requested.

Lui is cited in the Office Action as disclosing the use of an organic anti-reflective layer 85. Lui fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, and partially etching the inorganic filler filling the via and the organo silicate layer to form a trench, as claimed in claims 1-20. Lui further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 21-38. Lui further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, and partially etching the HSQ-based filler filling the via and the organo silicate layer to form a trench, as claimed in claims 39-52.

Lui, like Tsu, *et al.*, Aoi and Lee, *et al.*, fails to teach or suggest these elements of the invention set forth in claims 1-20, 21-28, and 39-52. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-20, 21-28, and 39-52. Therefore, it is believed that the claims 1-20, 21-28, and 39-52. are allowable over the cited references, and reconsideration of the rejections of claims 11-12, 14-15, 29-30, 32-33, 44 and 46-47 under 35 U.S.C. § 103(a) based on Tsu, *et al.*, Aoi, Lee, *et al.*, and Lui, is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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